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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/757,252	01/13/2004	Denise M. Eppich	MI22-2468	4388

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WELLS ST. JOHN P.S.
601 W. FIRST AVENUE, SUITE 1300
SPOKANE, WA 99201

EXAMINER	
FENTY, JESSE A	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 02/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

CT

Office Action Summary	Application No.	Applicant(s)	
	10/757,252	EPPICH ET AL.	
	Examiner	Art Unit	
	Jesse A. Fenty	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 November 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *69-81* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *69-81* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/18/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 69, 73, 74, and 76-81 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tonti et al. (U.S. Patent No. 6,436,749 B1) in view of Chau et al. (US 2003/0129793 A1).

In re claims 69, 73, 76 and 77, Tonti (Figs. 4, 4A) discloses a semiconductor device comprising:

A dielectric layer (10) over a substrate;

A PMOS gate (FET 36) and an NMOS gate (FET 34) over the dielectric layer;

A first metal-containing material (16) within the PMOS gate and over the dielectric layer, the first metal-containing material having a thickness of greater than 20 angstroms;

A second metal-containing material (16) within the NMOS gate and over the dielectric layer, the second metal-containing material having a thickness of less than or equal to about 20 angstroms;

A first layer of n-type doped silicon within the PMOS gate and over the first metal-containing material; and

A second layer of n-type doped silicon within the NMOS gate and over the second metal-containing material.

Tonti discloses a tungsten-nitride metal-containing layer but does not expressly disclose the first metal containing layer having a thickness of greater than 20 angstroms nor the second metal containing layer having a thickness of less than or equal to 20 angstroms. Chau et al. (Fig. 3J) discloses a metal-containing layer (214) with a thickness ranging from 10 to 25 angstroms (section [0016], lines 7-8)[1]. It would have been obvious for one skilled in the art at the time of the invention to provide a layer as disclosed by Chau for the device of Tonti for the purpose, for example, of providing a layer thick enough to prevent impurities from diffusing into the gate dielectric layer, but thin enough as to not interfere with the function of the upper metallic layer (Chau; section [0016], lines 1-6).

In re claim 74, Tonti in view of Chau discloses the device of claim 73, wherein the first and second metal-containing materials predominantly comprise tungsten nitride, tantalum nitride and tungsten nitride (Tonti; column 3, lines 1-2; Chau, section [0027]).

In re claims 78-80, Tonti in view of Chau discloses the device of claim 69, but does not expressly disclose the second thickness being on the order of 100 or 150 angstroms. Chau, however, does disclose the desirability of using thicker diffusion barrier layers (section [0016]) for the purpose of blocking the diffusion of impurities into the gate dielectric layer. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use a thicker diffusion barrier for the first metal-containing layer since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233.

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[1] This thickness dimension satisfied both limitations. The thickness for the first FET is disclosed to be greater than 20 angstroms, and the thickness for the second FET is disclosed to be greater than 20 angstroms.

In re claim 81, Tonti in view of Chau discloses the device of claim 69, wherein the semiconductor device is a part of an electronic system (Tonti; Summary of the Invention).

3. Claims 70-72 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tonti/Chau as applied to claim 1 above, and further in view of Taylor, Jr. et al. (U.S. Patent No. 6,573,160 B2).

In re claims 70-72, Tonti in view of Chau disclose the device of claim 1 but does not expressly disclose the gate oxide layer comprising aluminum oxide. Taylor discloses the use of aluminum oxide and hafnium oxide (column 3, lines 57-67) as gate dielectric layer alternatives. It would have been obvious for one skilled in the art at the time of the invention to use a thin high-dielectric constant oxide as disclosed by Taylor for the device of Tonti/Chau for the purpose, for example, of increasing the capacitance of the device (Taylor; column 1, lines 23-30).

4. Claim 75 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tonti/Chau as applied to claim 73 above, and further in view of Lee (U.S. Patent No. 6,306,743 B1).

In re claim 75, Tonti in view of Chau discloses the device of claim 73, but does not expressly disclose the first and second metal-containing materials comprising tungsten silicide. Lee discloses a gate structure (29) comprising a tungsten silicide layer (25). It would have been obvious for one skilled in the art at the time of the invention to use a tungsten silicide layer as disclosed by Lee for the device of Tonti/Chau for the purpose, for example, of decreasing the resistance of the gate electrode.

Response to Arguments

5. Applicant's arguments filed 11/18/04 have been fully considered but they are not persuasive.

a. Applicant argues (pp. 9) that since the primary reference, Tonti ('749), utilizes a common metal layer in the fabrication of NMOS and PMOS devices, "[a]ny processing which would be included in Tonti to form the metal containing material (16) to have a different thickness over the NMOS regions than over the PMOS regions would impose additional processing steps, which would reduce the efficiency of the Tonti process." However, the subject claims are not drawn to the method of making; the claims are drawn to the structure itself. Unless Tonti's method of making this structure is the only way to do so, the method of fabricating the structure does not preclude the combination of references if the motivation to do so is in the prior art. An alternative method of formation of the metal-containing layers and the CMOS transistors of Tonti is through selective deposition. Since the NMOS and PMOS regions of Tonti could be fabricated by a different method and still achieve the same final structure, the disclosed method of forming does not preclude the obviousness of the combined product and the combination of the references.

b. The secondary reference is relied upon for the motivation to combine the thin layer of Chau ('793) with the given metal-containing layer of Tonti. Applicant argues (pp. 10) that the Examiner "is incorrect to assume that [the teachings of Chau] imply a motivation to utilize metal-containing materials within the CMOS structures of Chau having different thicknesses in PMOS regions than in NMOS regions." This element is

broken down into two parts: the motivation to combine and the NMOS/PMOS layers having different thicknesses.

i. First, the motivation to use the Chau teachings in combination with that of Tonti stems from the similarity of the metal-containing materials of both references. Both references disclosed doped metal-containing layers above underlying layers. The Chau reference is used to enhance the structure of Tonti by providing an additional metal-containing layer (214) to prevent impurities from the second metal layer (216) from diffusing completely into the lower gate dielectric layer (Chau; section [0016]).

ii. Secondly, Applicant is concerned that Chau does not disclose using different thicknesses for the layer (214) for each of the NMOS and PMOS devices. On the contrary, Chau clearly discloses that the layer (214) "should be approximately 10 to 25 angstroms in thickness." Since the device of Chau is a CMOS device, the disclosed thickness is available for both the PMOS and NMOS transistors alike.

Therefore the disclosed references, in combination, read on the subject claims.

Conclusion

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO

MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jesse A. Fenty whose telephone number is 571-272-1729. The examiner can normally be reached on 5/4-9 1st Fri. Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 571-272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jesse A. Fenty
Examiner
Art Unit 2815

Tom Thomas

TOM THOMAS
SUPERVISORY PATENT EXAMINER